PGDCA Semester – I March 2015

25703 Paper No - 103. Logical Organization of Computer

Time : 03 Hours Marks : 100

Q-1 Answer the following questions in brief 20

1. Give the Full form of ALU , MICR
2. What do you mean by cache memory
3. Give the name of type of Flip-flop
4. One KB =.....Bits
5. Explain terms: Volatile memory and non Volatile memory
6. Convert into Hexadecimal: $(111111)_{10}$
7. Define : Computer
8. $(152)_{10} = (.....?.....)_2$
9. List out any three input and output devices.
10. What is the function of control unit and ALU?

OR

Q-1 Answer the following questions in brief 20

1. What is ASCII Code?
2. What is the use of Flash memory?
3. What is Counter?
4. What is Boolean algebra?
5. Give truth table of XOR and XNOR gate.
6. What is the use of Parity bit?
7. Define Truth table
8. Which gates are known as universal gates?
9. What is Arithmetic circuit? Give any three name of arithmetic circuit.
10. Define : Pipeline

Q-2 Answer the following questions 20

1. Explain CPU Organization in detail
2. Give the difference between Impact Printer and Non Impact Printer
3. State and prove De Morgan's Law
4. Explain Half adder with circuit

OR

Q-2 Answer the following questions 20

1. Write as short note on Instruction Execution Cycle
2. Write note on I/O Devices.
3. Explain Half Subtractor in detail
4. Give steps to convert from SOP to POS? Give Difference between SOP and POS.

Q-3 Answer the following questions 20

1. Explain IC in detail
2. Explain Encoder with diagram
3. Preparing a Truth Table using Circuit : F1=X+Y'+Z'

4. Explain CRT with diagram

OR

Q-3 Answer the following questions 20

1. Explain BCD Counter.
2. Write note on I/O Devices.
3. Explain T Flip Flop
4. Explain Multiplexer in detail

Q-4 Attempt the following 20

1. Explain Fundamental Gates
2. Explain RS flip-flop
3. Explain minterms and Maxterms
4. Explain 3 to 8 Line Decoder

OR

Q-4 Attempt the following 20

1. What do you mean Register? Explain parallel Register
2. Simplify function and Draw circuit :
   F = ABC'D + ABCD' + ABC'D'+ ABCD + A'B'C'D'
3. Explain Bus Arbitration in Detail
4. Explain 1 bit – 4 line demultiplexer

Q-5 [A] Do as Directed 16

1. $(1001111)_2=(?)_{10}$
2. $(746)_8=(?)_2$
3. $(101101)_2=(?)_{16}$
4. $(8291)_{10}=(?)_{16}$
5. $(9AF)_{16}=(?)_2$
6. $(1089)_{10}=(?)_2$
7. $(AF12)_{16}=(?)_{10}$
8. $(1000.100)_2-(1.1)_2$

[B] Draw Circuit $F=X'Y'Z+X'YZ+XY'$ 04

OR

Q-5 [A] Do as Directed 16

1. $(11011)_2+(1111)_2$	2. $(741)_{10}=(?)_2$
3. $(AFCA)_{16}=(?)_2$	4. $(11011010)/(101)$
5. $(1011.101) * (11)$	6. $(1111111.10111)_2=(?)_8$
7. $(6354)_8 = (?)_{16}$	8. 2's Compliment of $(11001)_2$

[B] Draw Circuit $F = [(A + B) . (A' + B')] + AB'C$ 04